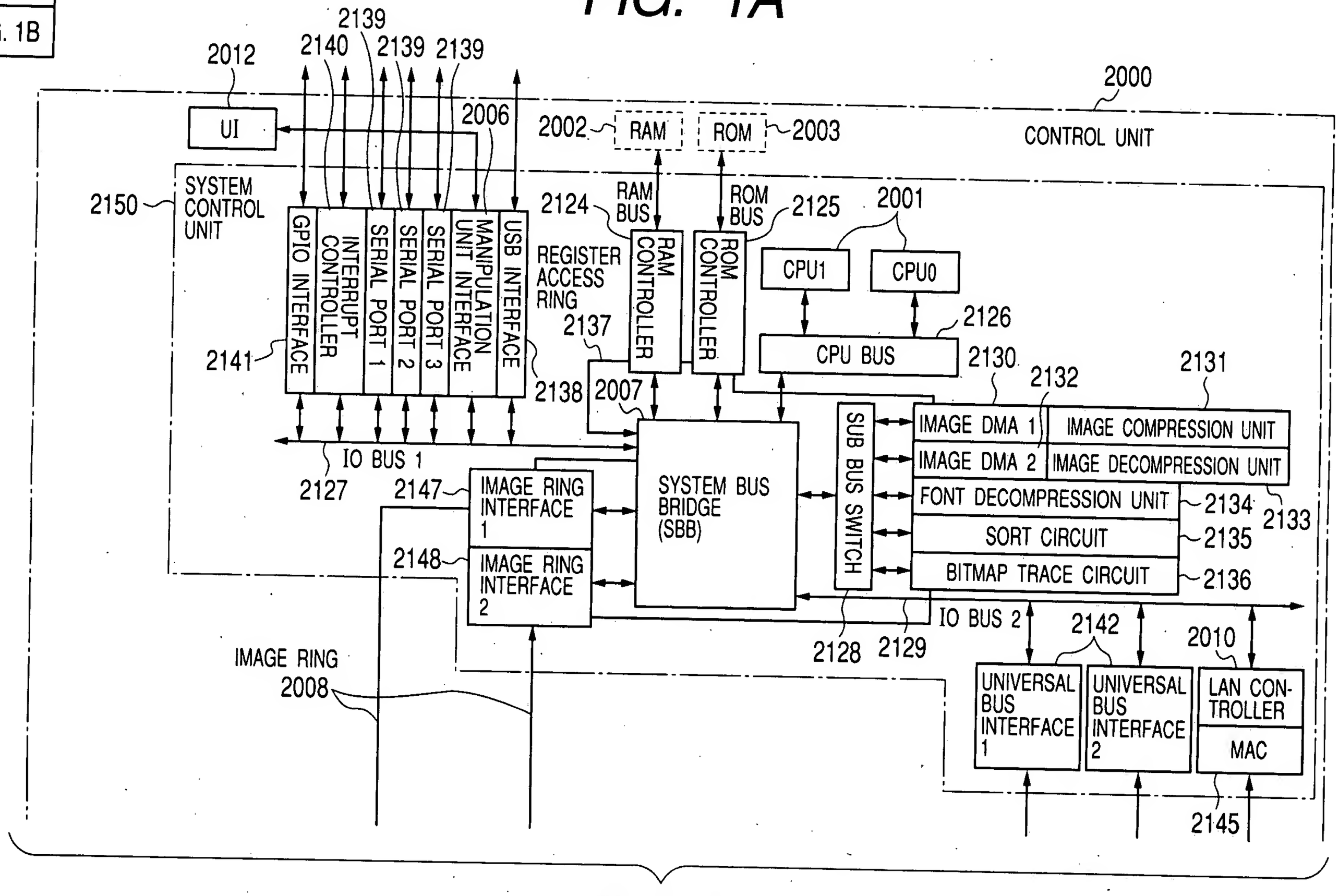
FIG. 1

FIG. 1A

FIG. 1B

FIG. 1A



TO FIG. 1B

FIG. 1B

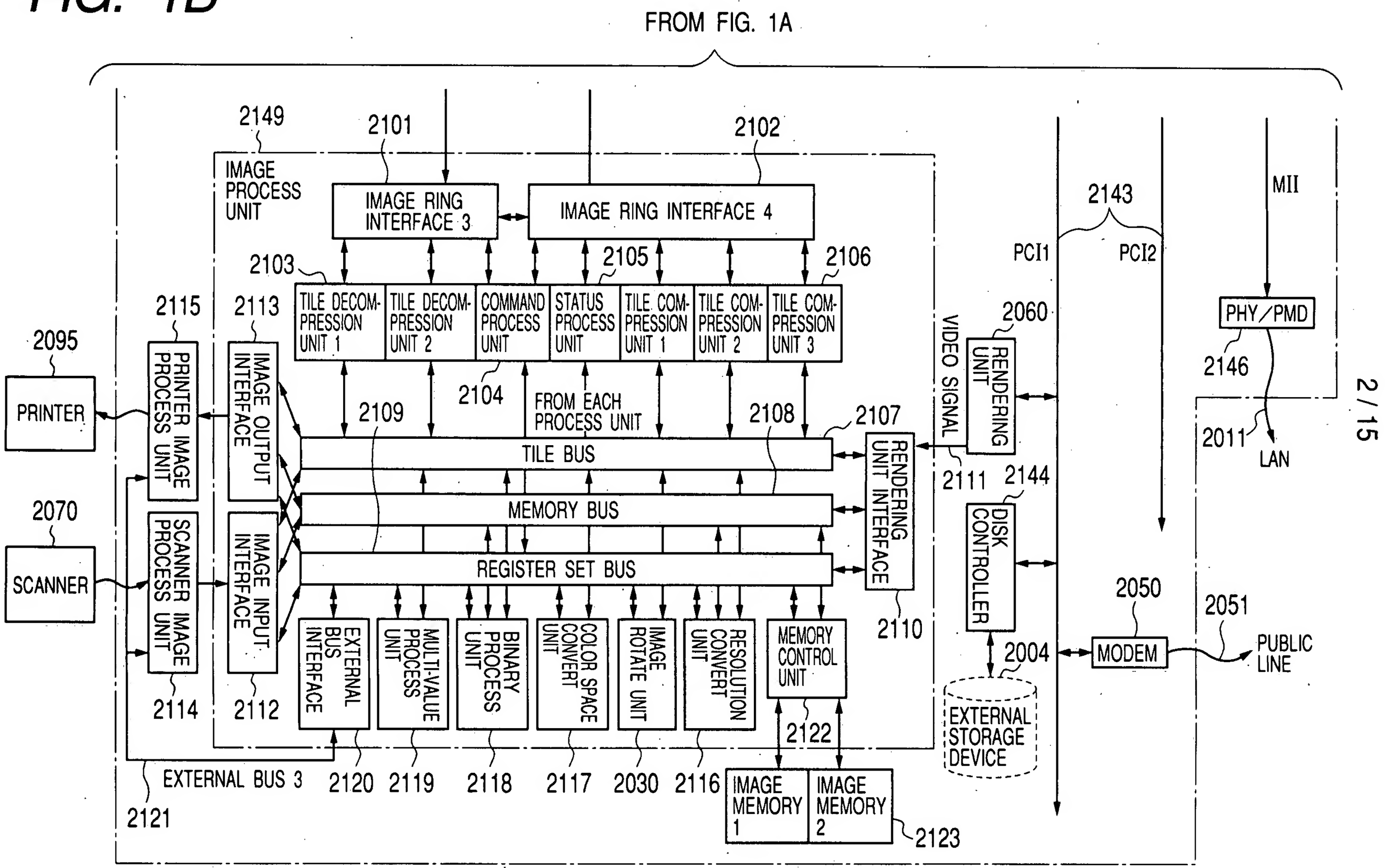

FROM FIG. 1A
2149
2101
2102
IMAGE PROCESS UNIT
IMAGE RING INTERFACE 3
IMAGE RING INTERFACE 4
2103
2105
2106
2115
2113
2095
TILE DECOM-PRESSION UNIT 1
TILE DECOM-PRESSION UNIT 2
COMMAND PROCESS UNIT
STATUS PROCESS UNIT
TILE COM-PRESSION UNIT 1
TILE COM-PRESSION UNIT 2
TILE COM-PRESSION UNIT 3
2104
FROM EACH PROCESS UNIT
2109
2108
2107
PRINTER
PRINTER IMAGE PROCESS UNIT
IMAGE OUTPUT INTERFACE
TILE BUS
MEMORY BUS
REGISTER SET BUS
RENDERING UNIT INTERFACE
2110
2111
VIDEO SIGNAL
RENDERING UNIT
2060
2143
PCI1
PCI2
MII
PHY/PMD
2146
2011
LAN
2144
DISK CONTROLLER
2070
SCANNER
SCANNER IMAGE PROCESS UNIT
IMAGE INPUT INTERFACE
2114
2112
EXTERNAL BUS INTERFACE
MULTI-VALUE PROCESS UNIT
BINARY PROCESS UNIT
COLOR SPACE CONVERT UNIT
IMAGE ROTATE UNIT
RESOLUTION CONVERT UNIT
MEMORY CONTROL UNIT
2122
2050
2051
MODEM
PUBLIC LINE
2004
EXTERNAL STORAGE DEVICE
EXTERNAL BUS 3
2121
2120
2119
2118
2117
2030
2116
IMAGE MEMORY 1
IMAGE MEMORY 2
2123

FIG. 2

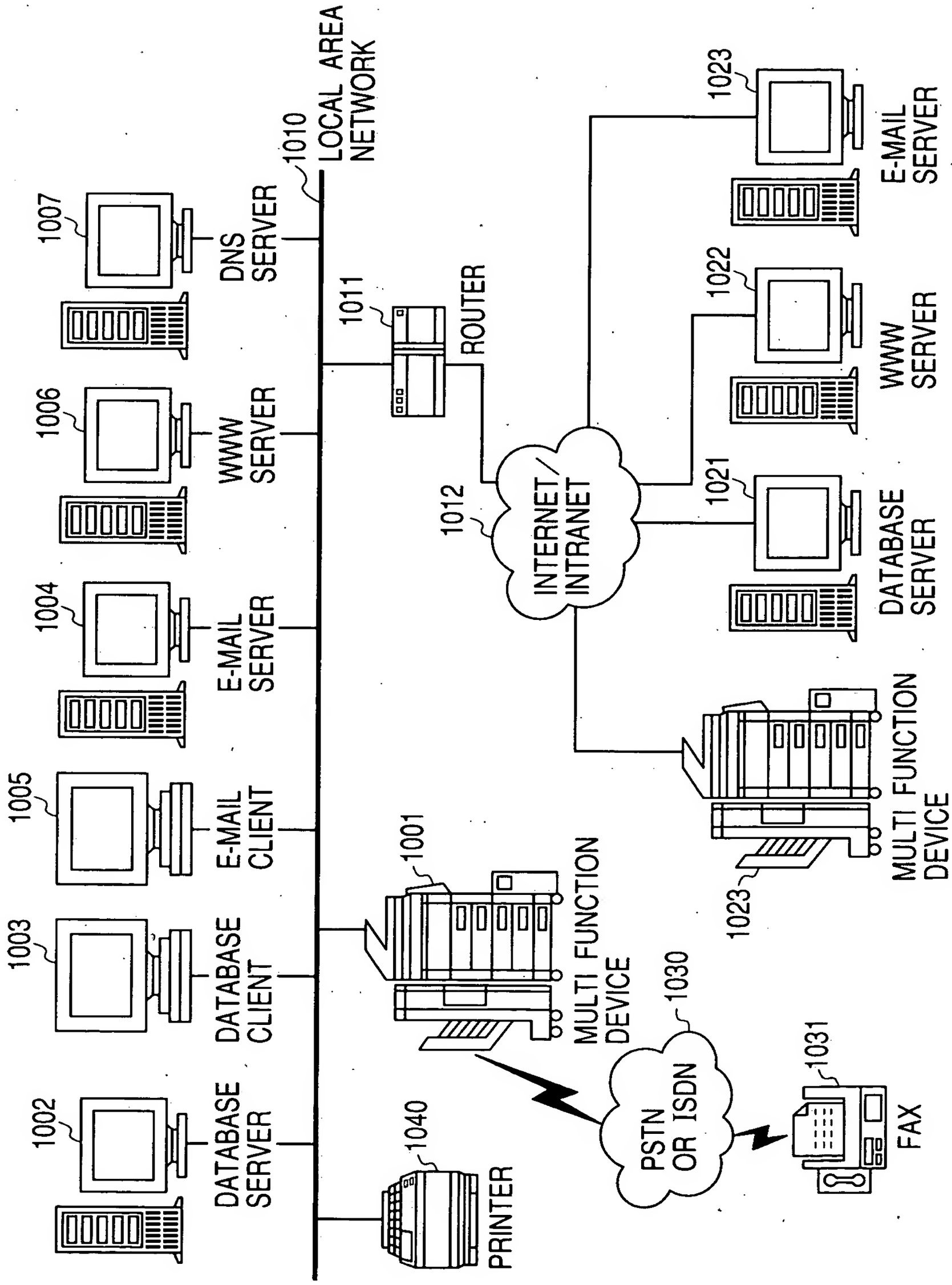
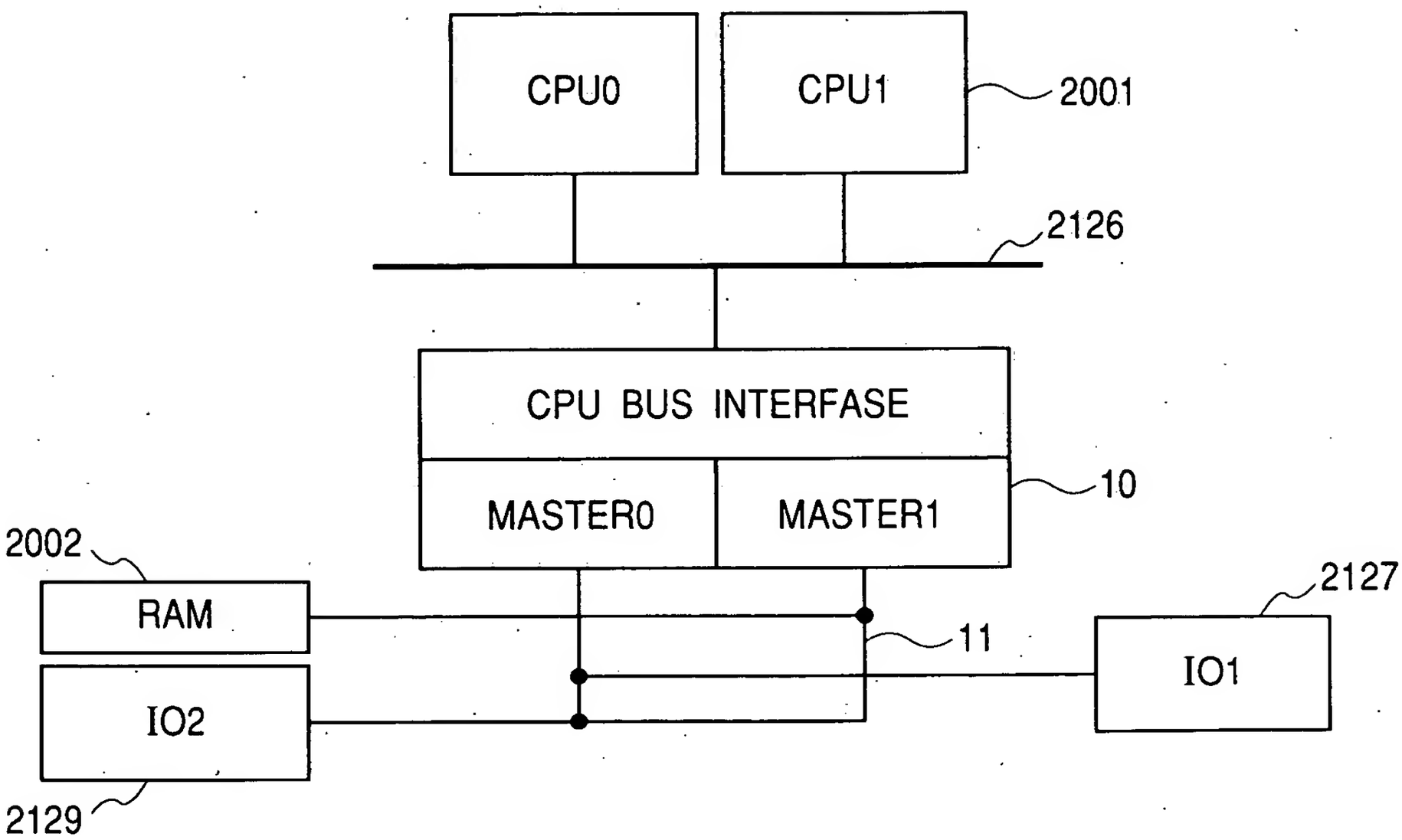

1010
LOCAL AREA NETWORK
1007
DNS SERVER
1006
WWW SERVER
1004
E-MAIL SERVER
1005
E-MAIL CLIENT
1003
DATABASE CLIENT
1002
DATABASE SERVER
1001
1040
PRINTER
1011
ROUTER
1012
INTERNET / INTRANET
1023
E-MAIL SERVER
1022
WWW SERVER
1021
DATABASE SERVER
MULTI FUNCTION DEVICE
1030
PSTN OR ISDN
1031
FAX

FIG. 3


CPU0
CPU1
2001
2126
CPU BUS INTERFASE
MASTER0
MASTER1
10
2002
RAM
IO2
2129
11
2127
IO1

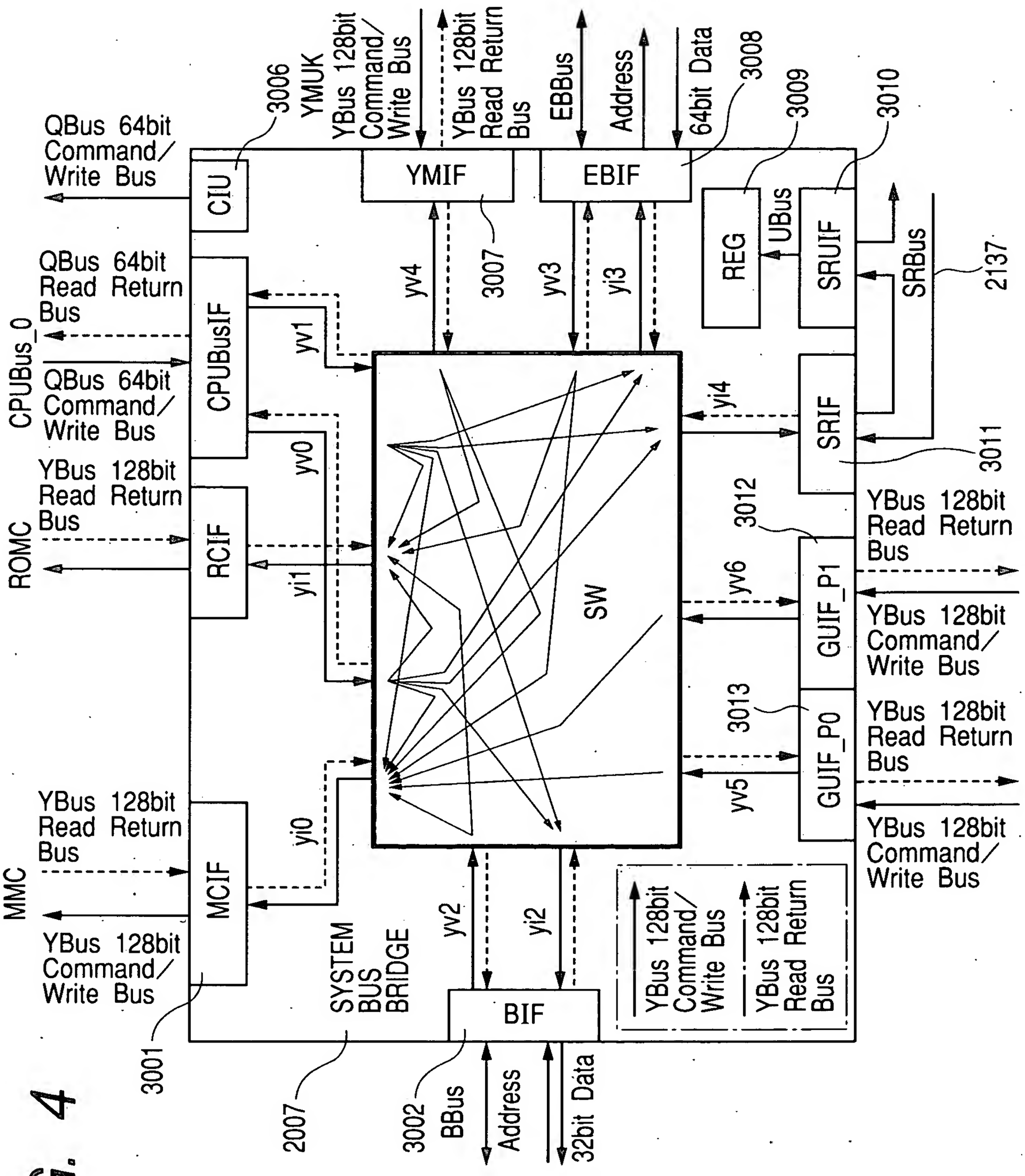

QBus 64bit Command/ Write Bus
QBus 64bit Read Return Bus
CPUBus_0
QBus 64bit Command/ Write Bus
YBus 128bit Read Return Bus
ROMC
YBus 128bit Read Return Bus
MMC
YBus 128bit Command/ Write Bus
3001
CIU
CPUBusIF
RCIF
MCIF
3006
YMUK
YBus 128bit Command/ Write Bus
YBus 128bit Read Return Bus
EBBus
Address
64bit Data
3008
3009
3010
YMIF
EBIF
REG
UBus
SRUIF
SRBus
2137
yv4
3007
yv3
yi3
yv1
yv0
yi1
yi0
SW
yi4
SRIF
3011
3012
yv6
GUIF_P1
YBus 128bit Read Return Bus
YBus 128bit Command/ Write Bus
3013
yv5
GUIF_P0
YBus 128bit Read Return Bus
YBus 128bit Command/ Write Bus
SYSTEM BUS BRIDGE
2007
yv2
yi2
BIF
3002
BBus
Address
32bit Data
YBus 128bit Command/ Write Bus
YBus 128bit Read Return Bus

FIG. 4

FIG. 5

FIG. 5A	FIG. 5B

FIG. 5A

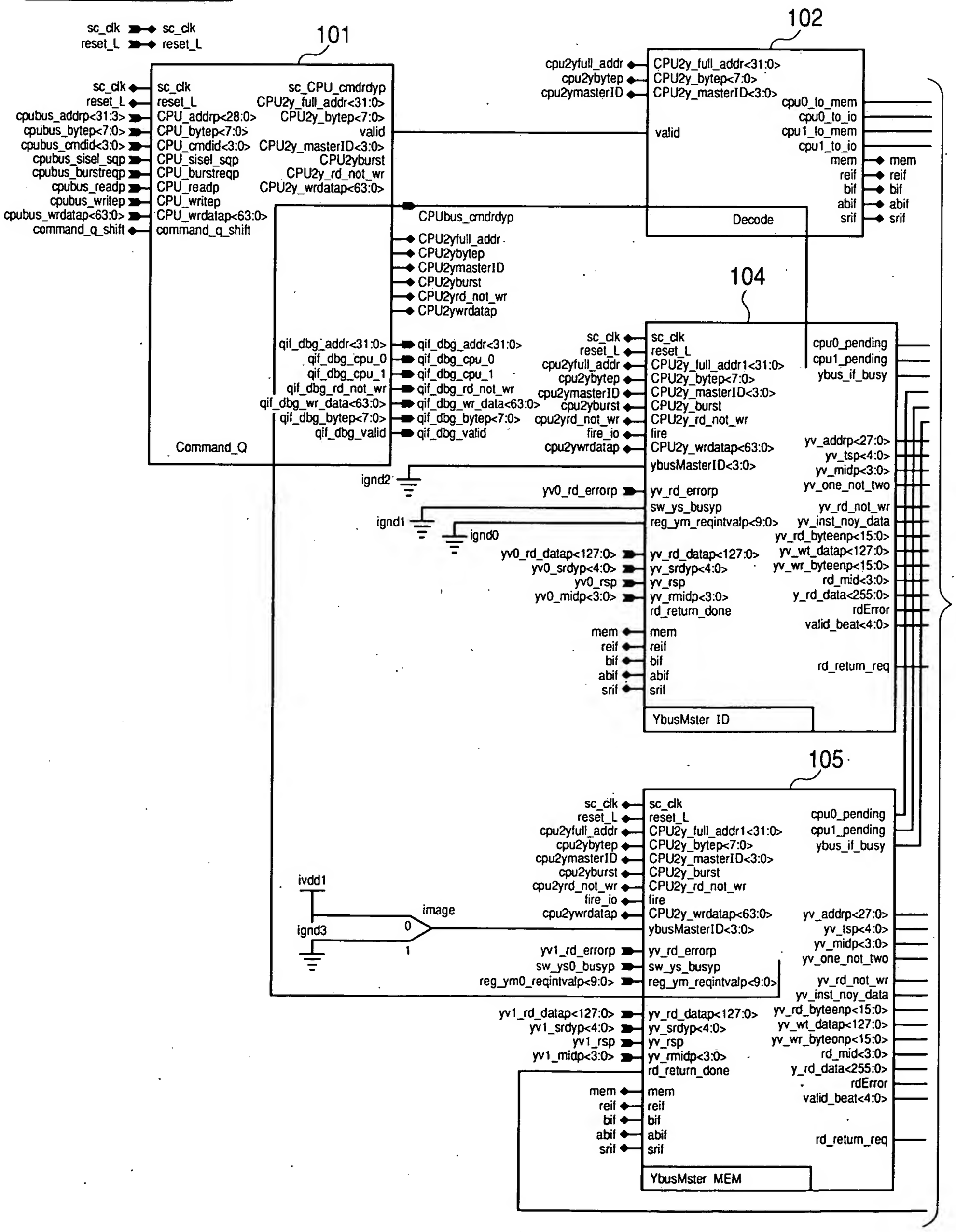


FIG. 5B

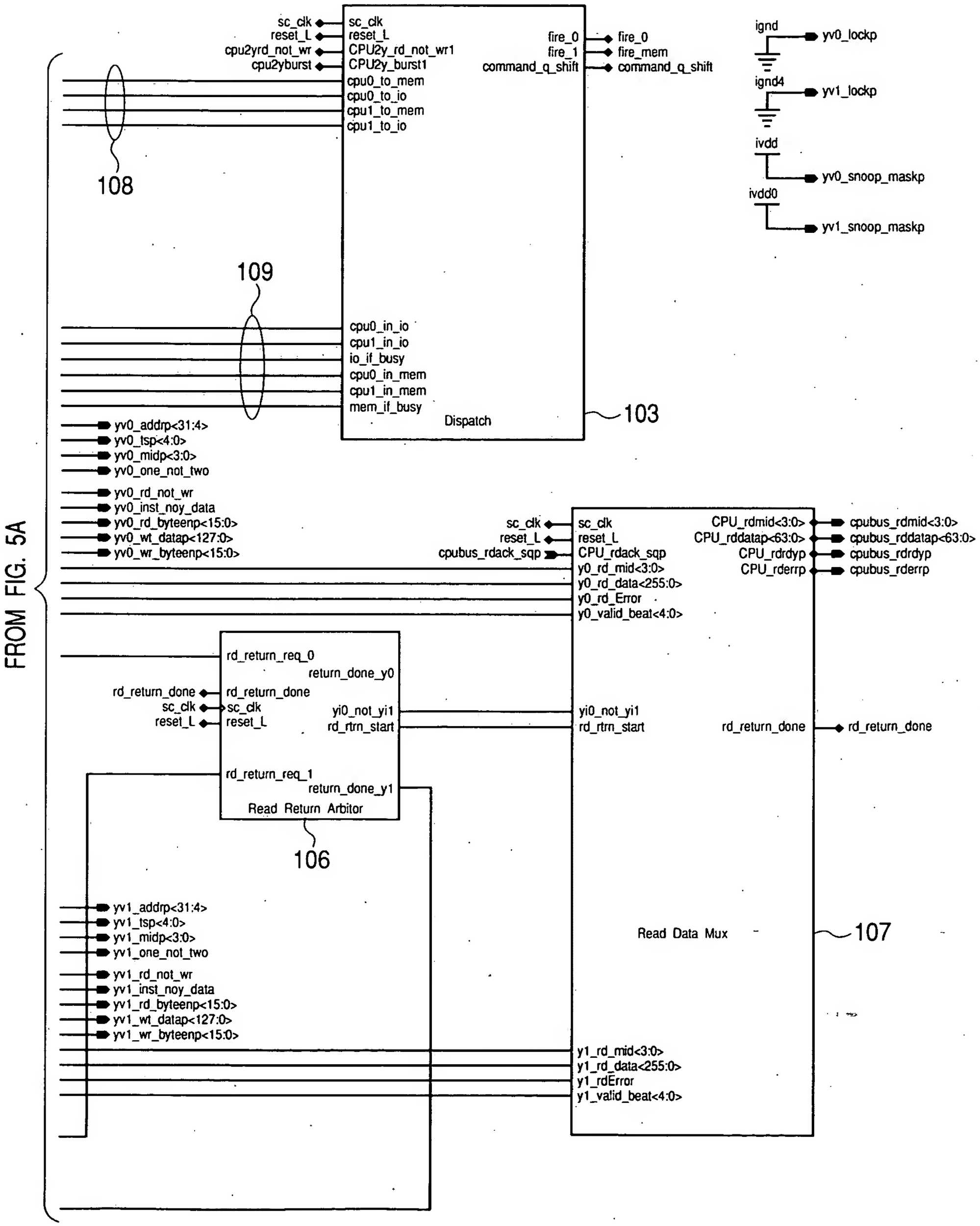

FROM FIG. 5A
108
109
sc_clk
reset_L
cpu2yrd_not_wr
cpu2yburst
CPU2y_rd_not_wr1
CPU2y_burst1
cpu0_to_mem
cpu0_to_io
cpu1_to_mem
cpu1_to_io
fire_0
fire_1
command_q_shift
ignd
yv0_lockp
ignd4
yv1_lockp
ivdd
yv0_snoop_maskp
ivdd0
yv1_snoop_maskp
cpu0_in_io
cpu1_in_io
io_if_busy
cpu0_in_mem
cpu1_in_mem
mem_if_busy
Dispatch
103
yv0_addrp<31:4>
yv0_tsp<4:0>
yv0_midp<3:0>
yv0_one_not_two
yv0_rd_not_wr
yv0_inst_noy_data
yv0_rd_byteenp<15:0>
yv0_wt_datap<127:0>
yv0_wr_byteenp<15:0>
cpubus_rdack_sqp
y0_rd_mid<3:0>
y0_rd_data<255:0>
y0_rd_Error
y0_valid_beat<4:0>
CPU_rdmid<3:0>
CPU_rddatap<63:0>
CPU_rdrdyp
CPU_rderrp
cpubus_rdmid<3:0>
cpubus_rddatap<63:0>
cpubus_rdrdyp
cpubus_rderrp
rd_return_req_0
return_done_y0
rd_return_done
yi0_not_yi1
rd_rtrn_start
rd_return_req_1
return_done_y1
Read Return Arbitor
106
yv1_addrp<31:4>
yv1_tsp<4:0>
yv1_midp<3:0>
yv1_one_not_two
yv1_rd_not_wr
yv1_inst_noy_data
yv1_rd_byteenp<15:0>
yv1_wt_datap<127:0>
yv1_wr_byteenp<15:0>
y1_rd_mid<3:0>
y1_rd_data<255:0>
y1_rdError
y1_valid_beat<4:0>
Read Data Mux
107

FIG. 6

Transaction Type	Description	
Non-cached Instruction Read	Single read	
cached Instruction Read	4 beat burst read	Critical word first (CWF)
Non-cached Load Data Read	Single read	
cached Load Data Read	4 beat burst read	CWF
Store Data Write	Single write	
Store Data Write Burst	4 beat burst write	CWF

FIG. 7

LAST SOURCE	LAST TARGET	CURRENT SOURCE	CURRENT TARGET	ISSUE PERMISSION
CPU0	IO A	CPU0	IO A	○
CPU0	IO A	CPU0	OTHER THAN IO A	×
CPU0	IO A	CPU0	MEM	×
CPU0	IO A	CPU1	IO A	○
CPU0	IO A	CPU1	OTHER THAN IO A	×
CPU0	IO A	CPU1	MEM	○
CPU0	MEM	CPU0	IO	×
CPU0	MEM	CPU0	MEM	○
CPU0	MEM	CPU1	IO	○
CPU0	MEM	CPU1	MEM	○
CPU1 (INVERSE AS WELL)				

FIG. 8

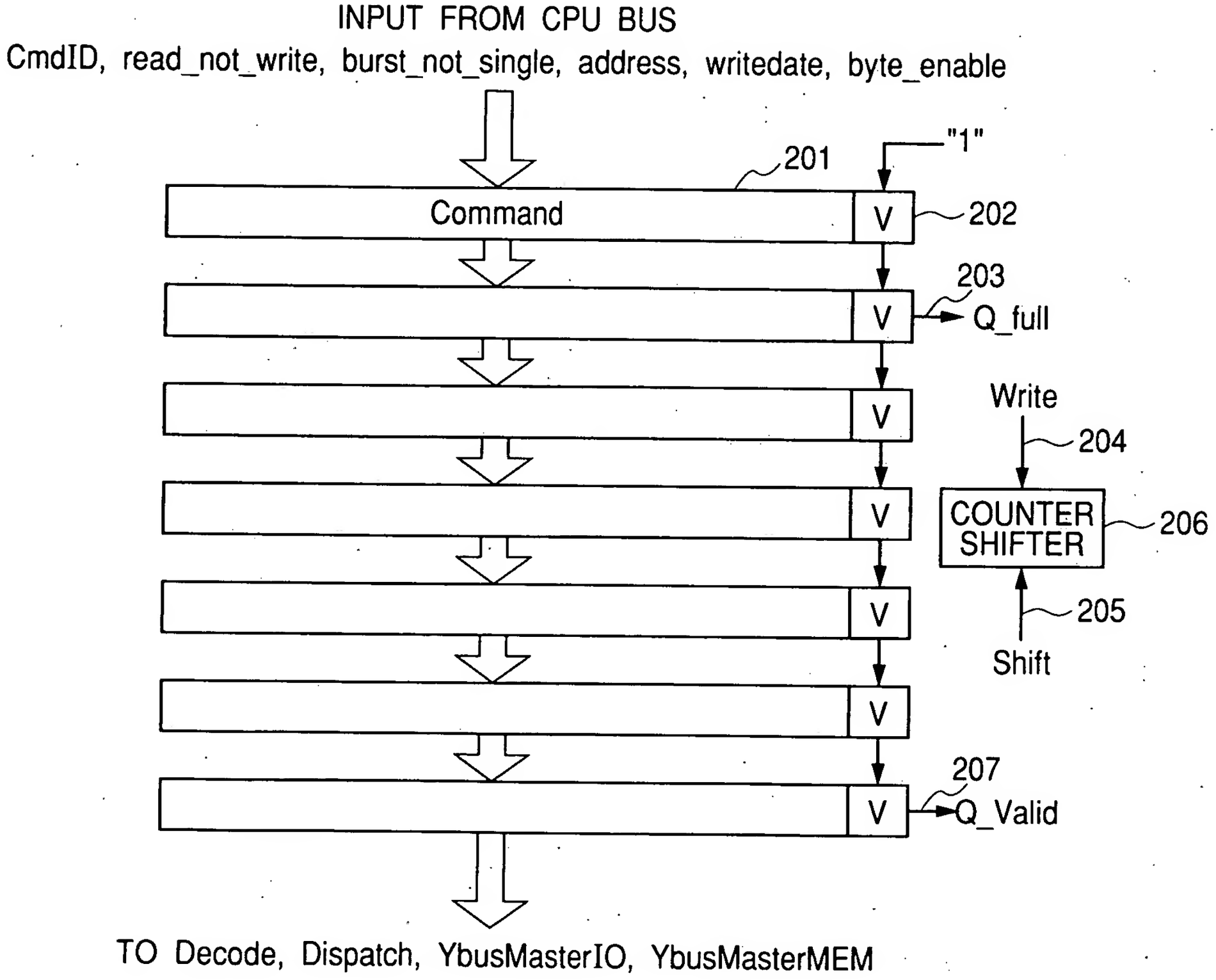

INPUT FROM CPU BUS
CmdID, read_not_write, burst_not_single, address, writedate, byte_enable
"1"
201
Command
V
202
203
V
Q_full
Write
204
COUNTER
SHIFTER
206
205
Shift
207
Q_Valid
TO Decode, Dispatch, YbusMasterIO, YbusMasterMEM

FIG. 9

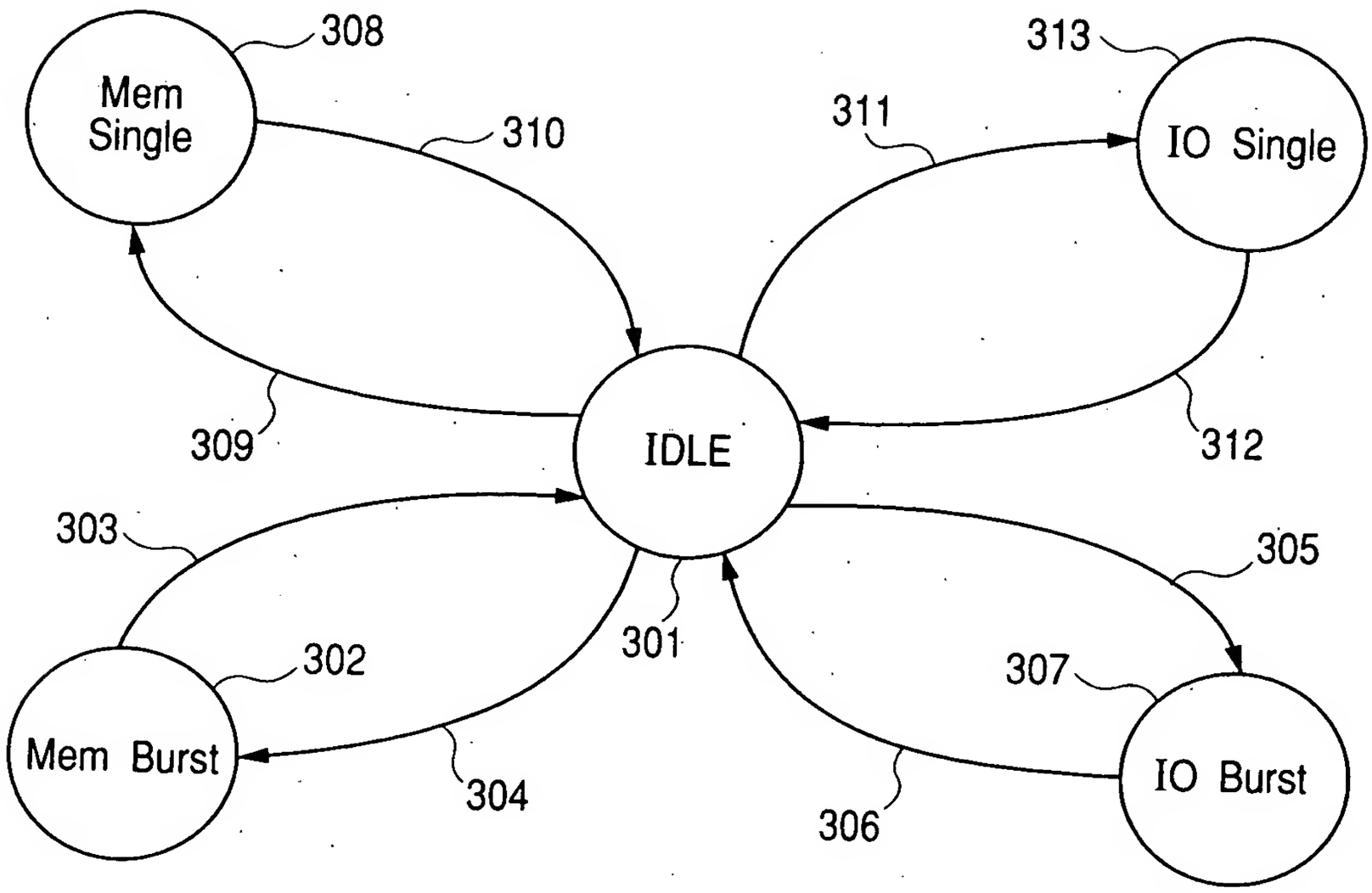

Mem Single
308
310
309
313
311
IO Single
312
IDLE
303
302
Mem Burst
304
301
305
307
IO Burst
306

FIG. 10

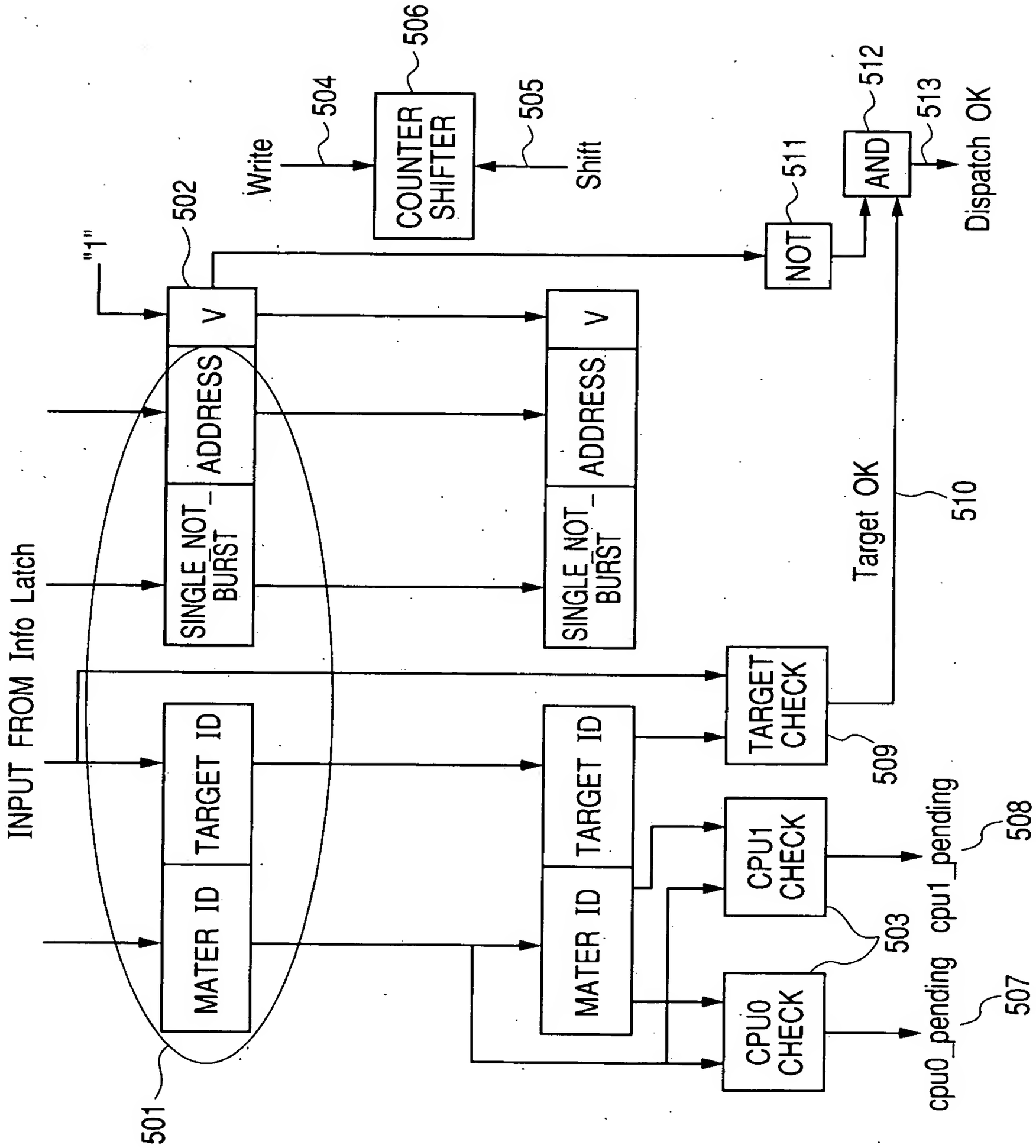

INPUT FROM Info Latch
"1"
502
V
ADDRESS
SINGLE_NOT_BURST
TARGET ID
MATER ID
501
Write
504
COUNTER
506
Shift
505
NOT
511
AND
512
Dispatch OK
513
Target OK
510
TARGET CHECK
509
CPU1 CHECK
cpu1_pending
508
503
CPU0 CHECK
cpu0_pending
507

FIG. 11

FIG. 11A

FIG. 11B

FIG. 11A

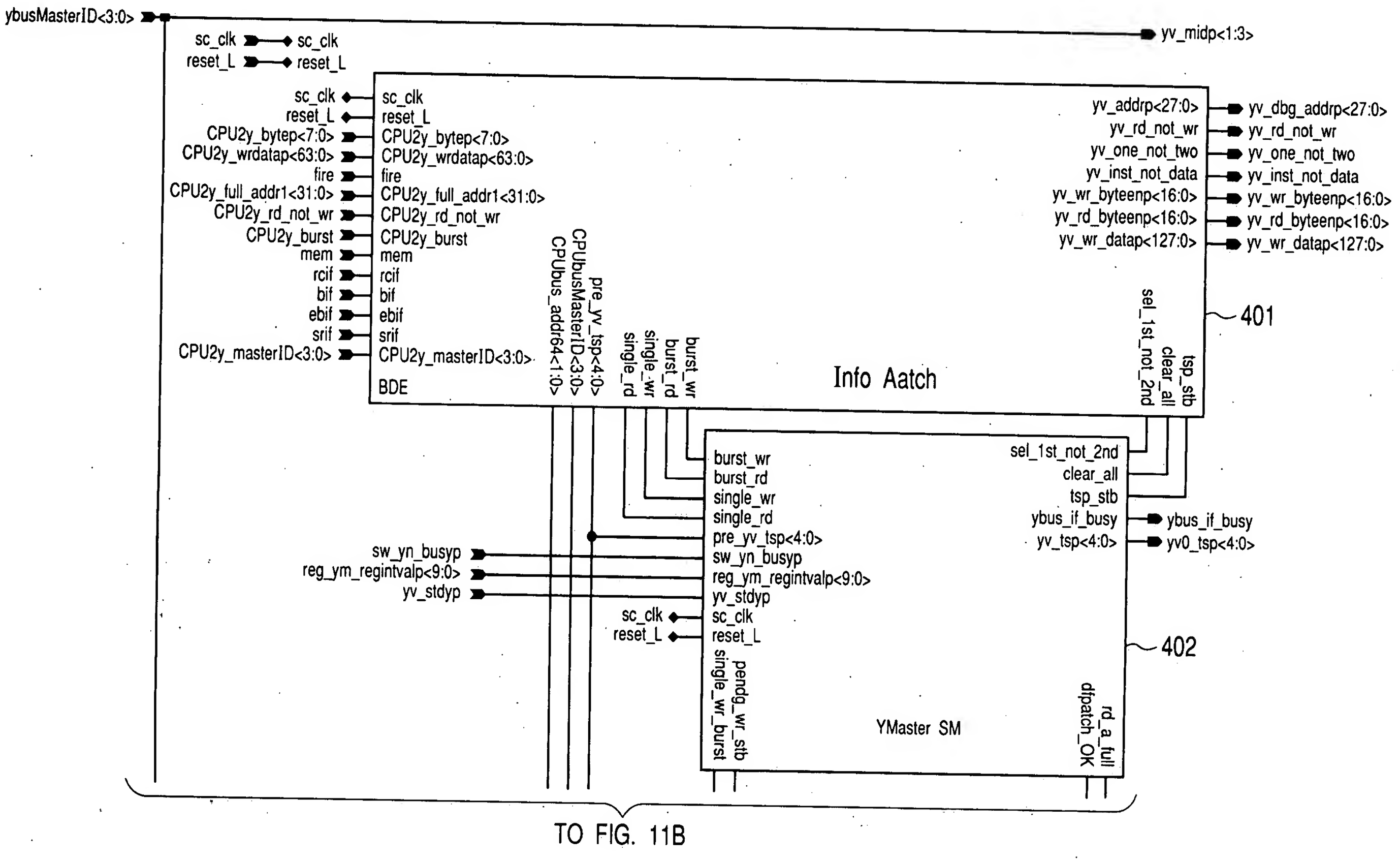


FIG. 11B

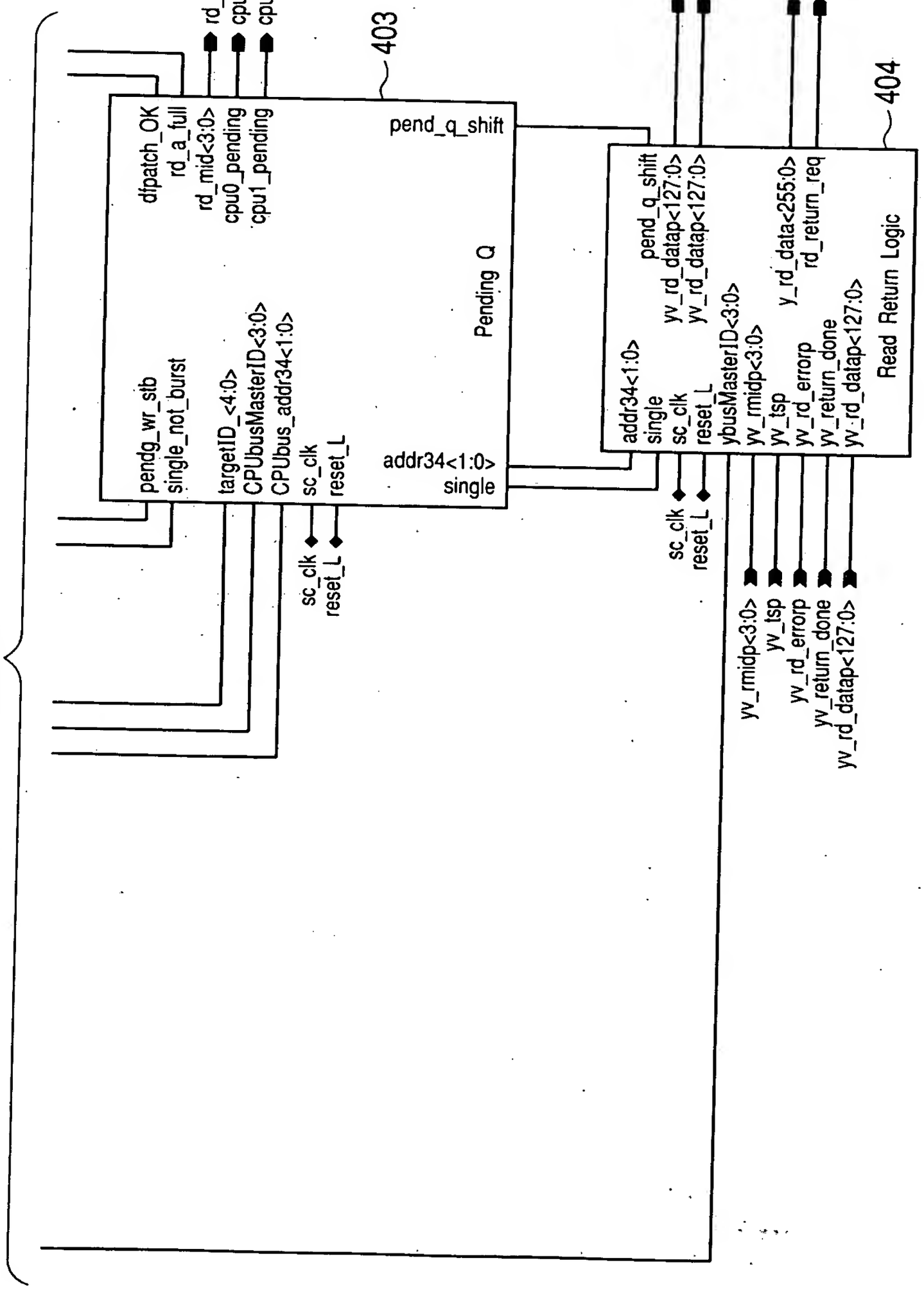

FROM FIG. 11A
403
404
rd_mid<3:0>
cpu0_pending
cpu1_pending
dtpatch_OK
rd_a_full
rd_mid<3:0>
cpu0_pending
cpu1_pending
pend_q_shift
pendg_wr_stb
single_not_burst
targetID_<4:0>
CPUbusMasterID<3:0>
CPUbus_addr34<1:0>
sc_clk
reset_L
Pending Q
addr34<1:0>
single
sc_clk
reset_L
rdError
valid_beat<4:0>
y_rd_data<255:0>
rd_return_req
addr34<1:0>
single
sc_clk
reset_L
pend_q_shift
yv_rd_datap<127:0>
yv_rd_datap<127:0>
ybusMasterID<3:0>
yv_rmidp<3:0>
yv_tsp
yv_rd_errorp
yv_return_done
yv_rd_datap<127:0>
y_rd_data<255:0>
rd_return_req
Read Return Logic
sc_clk
reset_L
yv_rmidp<3:0>
yv_tsp
yv_rd_errorp
yv_return_done
yv_rd_datap<127:0>

FIG. 12
PRIOR ART